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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,408	07/16/2001	Sheng Hsiung Chen	TS01-133	3764

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EXAMINER	
BERRY, RENEE R	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,408	CHEN ET AL.	
	Examiner	Art Unit	
	Renee R Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,117,725 to Huang.

In regards to claim 1, Huang teaches a method of creating metal gate electrodes and polysilicon gate electrodes over the surface of substrate, said metal gate electrodes and said polysilicon gate electrodes having gate dielectric layers of different thickness, comprising the steps of: providing a semiconductor substrate, at least one first and one second gate electrode structures having been provided over the surface of said substrate, said at least one first and said at least one second gate electrode having been provided with a gate electrode body having a surface further having sidewalls which are essentially perpendicular the surface of said substrates said at least one first and said at least one second gate electrode having been provided with Doped impurity implants into the surface of said substrate that are self-aligned with the body of said at least one first and said at least one second gate electrode, said at least one first and

said at least one second gate electrode having been provided with gate spacers over said sidewalls of said at least one first and said at least one second gate electrode, said at least one first and said at least one second gate electrode having source and drain impurity implants into substrate that are self-aligned with the gate spacers of said at least one first and said least one second gate electrodes said been provided with the surface of said at least one first and said at least one second gate electrode being imbedded in layer of IMD having been polished down to the surface the body of said at least one first and said at least one second gate electrode, said at least one first and said at least one second gate electrode being electrically isolated from each other by region of Field Isolation that has been created in the surface said substrate; layer of Intra Metal Dielectric (IMD), said creating a photo-resist mask overlying said at least one second gate electrode; removing said dummy gate electrode from between said gate spacers of said least one first gate electrode, creating at least one opening said layer of IMD; depositing layer of high-k dielectric over the surface of said layer of IMD, including inside surfaces of said at least one opening created said layer of IMD; depositing a layer of metal over the surface of said layer of high-k dielectric, filling said at least said layer of IMD; and one opening created removing said layer of high-k dielectric and said layer metal from above the surface of said layer of IMD, leaving said layer of high-k dielectric in place over inside surfaces of said at least one opening created said layer of IMD, further leaving said layer of metal place over the surface of said layer of high-k dielectric inside said at least one opening created in said layer of IMD at column 4, lines 18-33-47 and column 5, 42-53 and column 6, lines 34-40.

In regards to claim 2, Huang teaches layer of high-k dielectric deposited over the surface of said layer of IMD is deposited thickness between about 50 and 150 Angstrom and more preferably to a thickness about 100 Angstrom at column 5, lines 42-45.

In regards to claim 3, Huang teaches layer of high-k dielectric deposited over the surface of said layer of IMD is selected from the group consisting of silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3) and oxide-nitride-oxide (ONO) and silicon oxide (Si_2O) and tantalum pentoxide (TaO_5) and titanium oxide (TiO_2) and zirconium oxide (ZrO_2) and tantalum oxide (Ta_2O_5) and barium titanium oxide ($BaTiO_3$) and strontium titanium oxide ($SrTiO_3$) at column 5, lines 33-39.

In regards to claim 4, Huang teaches layer of metal deposited over the surface of said layer of high-k comprises a metal selected from the group consisting of titanium and tungsten and copper and aluminum and alloys thereof at column 5, lines 7-20.

In regards to claim 5, Huang teaches a gate wherein at least one first gate electrode comprises electrode body of said a patterned layer of gate dielectric created over the surface of said substrate over which a patterned layer of polysilicon has been created at column 4, lines 33-36 and column 7, lines 46-51, claim 1.

In regards to claim 6, Huang teaches a gate electrode body of said at least one second gate electrode comprises a patterned layer of gate dielectric deposited thickness between about 300 and 600 Angstrom and more preferably about 450 Angstrom over which patterned layer of polysilicon has been created at column 6, lines 25-36.

In regards to claim 7, Huang teaches an additional processing step of depositing a layer of barrier material over the surface of said layer of IMD, said additional processing step being performed prior to depositing said high-k dielectric over the surface of said layer of IMD, said layer of barrier material being removed from the surface of said layer of IMD as an extension of said step of removing said layer high-k dielectric and said layer of metal from above the surface of said layer of IMD, leaving said barrier material in place overlying inside surfaces of said at least one opening created in said layer if IMD at column 4, lines 18-33-47 and column 5, 42-53 and column 6, lines 34-40.

In regards to claim 8, Huang teaches with additional saliciding contact surfaces at least one second gate electrode, said salicidation being performed prior to said providing gate spacers over said processing steps of to said at least one first and said sidewalls of said at least one first and said at least one second gate electrode at column 4, lines 43-47.

In regards to claim 9, Huang teaches a method of creating at least one high voltage polysilicon gate electrode and one low voltage metal gate electrode over the surface of substrate, comprising the steps of: providing a semiconductor substrate; creating a region of Field Isolation in the surface of said substrate, thereby separating an active surface region in the surface of said substrate over which said at least one high-voltage gate electrode to be created from an active surface region in the surface one low-voltage metal gate electrode is said substrate over which said at least created; creating a layer of gate oxide over the surface of said substrate, said layer of gate oxide

having a thickness between about 300 and 600 Angstrom and more preferably about Angstrom; depositing a layer of polysilicon layer of gate oxide; over the surface said patterning and etching said layer of polysilicon and said layer of pad oxide, creating patterned layers polysilicon and gate oxide having sidewalls further having a surface for said least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode over the surface of a substrate; performing Lightly Doped Diffusion impurity implants into the surface of said substrate self-aligned with said patterned layers of polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode; sidewalls of said patterned layers of polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said least one low voltage metal gate electrode; performing source and drain impurity implants into the surface of said substrate self-aligned with said gate spacers created over sidewalls said patterned layers of polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode; creating gate spacers over saliciding the surface of said source and drain impurity implants and the surface of said patterned layers of polysilicon for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode, creating salicided contact surfaces said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode; depositing a layer of Intra Metal Dielectric over the surface of said substrate, including the salicided contact surfaces and the surface of said gate spacers created over sidewalls of said patterned layers of

polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode; polishing said deposited layer Intra Metal Dielectric down said salicided contact surfaces said patterned and salicided layers of polysilicon for said at least one high voltage polysilicon gate electrode and said at least one voltage metal gate electrode; creating a photoresist mask overlying the surface of said layer of Intra Metal Dielectric, said at least one high voltage said photoresist mask overlying polysilicon gate electrode; removing said at least one low voltage gate electrode from between said gate spacers formed over sidewalls of said layers of polysilicon and depositing a layer of metal over the surface of said layer of high-k dielectric, filling said at least one opening created said layer of IMD; and said layer of metal from above the surface of said layer of high-k dielectric in place over inside surfaces of said layer of IMD, leaving said at least one opening created leaving said layer of metal said layer place over the surface of said IMD, further removing said layer of high-k dielectric layer of high-k dielectric inside said at least one opening created said layer of IMD at column 4, lines 18-33-47 and column 5, 42-53 and column 6, lines 34-40.

In regards to claim 10, Huang teaches a layer of high-k dielectric deposited over the surface of said layer of IMD is deposited to thickness of between about 50 and 150 Angstrom and more preferably to a thickness of about 100 Angstrom at column 6, lines 34-39.

In regards to claim 11, Huang teaches a layer of high-k dielectric deposited over the group consisting of silicon nitride surface said layer of IMD is selected from

(Si_3N_4) and aluminum oxide (Al_2O_3) and oxide-nitride-oxide (ONO) and silicon oxide tantalum pentoxide (TaO_5) and titanium oxide oxide (ZrO_2) and tantalum oxide ($BaTiO_2$) and strontium titanium oxide ($SrTiO_3$), (TiO_2) and zirconium (Si_2O) and (Ta_2O_5) and barium titanium oxide at column 3, lines 65-66.

In regards to claim 12, Huang teaches a layer of metal deposited over the surface of said layer of high-k comprises a metal selected from the group consisting of titanium and tungsten and copper and aluminum and alloys thereof at column 6, lines 34-39.

In regards to claim 13, Huang teaches one high voltage polysilicon gate electrode comprises a patterned layer of gate dielectric deposited to a thickness between about 300 and 600 Angstrom and more preferably about 450 Angstrom over which patterned and salicided layer of polysilicon has been created.

In regards to claim 14, Huang teaches an additional processing step of depositing a layer of barrier material over surface of said layer of IMD, said additional processing step being performed prior to depositing said high-k dielectric over the surface of said layer of IMD, said layer of barrier material being removed from the surface of said layer of IMD as an extension of said step of removing said layer of metal from above the surface of high-k dielectric and said layer said layer of IMD, leaving said barrier material in place overlying inside surfaces of said least one opening created in said layer if IMD at column 5, lines 42-49.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

RRB
January 30, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800